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A Very Small Frequency Generator System for Spread Spectrum EHF Applications

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Abstract - This paper reports on a novel synthesizer architecture, utilizing a hybrid Direct Digital / Direct Analog approach, which was optimized for small size, fast tuning, low spurious and low phase noise for a hopping EHF terminal. Performance data of the completed Frequency Generator System is presented which shows 500 nanosecond frequency switching speeds over a 600 MHz tuning bandwidth centered at 11.1 GHz, with 2.2 Hz resolution. Single-sided phase noise, L(f), is less than -80 dBc/Hz at a 1 kHz offset from the 11 GHz output and the worst case spurious is -40 dBc. The complete unit was packaged in 72 cubic inches, weighs 3.0 pounds and requires 16.5 Watts of DC power during continuous operation. This frequency generator demonstrates a vast improvement over any other reported synthesizer implementations for EHF systems.

I. INTRODUCTION

New synthesizer architectures are required to meet the demands of modern spread spectrum EHF communications. The Terminal Technology group at Lincoln Laboratory has been involved specifically in the development of man-portable terminals which impose additional requirements on the electronics. Together these can be summarized by the following:

a) Broad bandwidth and high resolution.
b) Extremely fast frequency switching / settling rates.
c) Adequate spectral purity to prevent interference.
d) Small size, lightweight and low dc power consumption.

The first three goals are common to most EHF systems. The last set of goals are especially important for a man portable terminal.

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There are three basic approaches for designing a high resolution, frequency synthesizer that are in common use today. They are a) Indirect Synthesis incorporating a Voltage Controlled Oscillator (VCO) in a tunable Phase Lock Loop (PLL); b) Direct Analog Synthesis, which incorporates cascaded stages of mix and divide networks to generate a desired resolution or number of channels; and c) Direct Digital Synthesis, which uses digital accumulators, a ROM and a digital to analog converter (DAC). Many systems incorporate a mixture or hybrid of these designs in order to take advantage of the benefits of increased speed or improved resolution that one approach may have over another.

The synthesizer that is presented in this paper is a hybrid mix of Direct Digital and Direct Analog designs, resulting in a unique frequency generator system ideally suited for a man-portable EHF terminal.

II. SYNTHESIZER COMPARISONS

A - Indirect Synthesis

One of the primary disadvantages of Indirect / PLL synthesizers is their relatively slow tuning speeds. A basic limitation of any PLL is that its tuning speed is proportional to the inverse of the closed loop bandwidth. A narrow loop bandwidth is required to keep the loop locked and to reduce phase noise, while a wide loop bandwidth is desired for fast tuning. In order to change output frequencies at the rate required for the EHF waveform, this class of synthesizer typically requires significant added circuitry.[1] A common solution to achieving the fast hopping requirement is to incorporate two independent PLL's whose outputs are time-multiplexed into the remaining rf hardware. The reason for this ping-pong" arrangement is to insure that each PLL has sufficient time to tune to a new frequency and settle before its output signal is used.

Sometimes a Phase Lock Loop synthesizer may incorporate a direct digital synthesizer in its reference circuitry in order to increase resolution or to reduce its switching speed. A major drawback of this approach is that the PLL acts as a multiplier on any phase noise or spurious in its reference and a DDS can have relatively high spurious. The resulting noise at the PLL output can seriously degrade system performance.[2]

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B - Direct Analog Synthesis

Another common synthesizer design is the direct analog synthesizer. By cascading stages of multipliers, dividers and mixers, a large number of separate frequencies or channels, can be generated from a single reference. The desired output signal can be rapidly switched between any set of frequencies at very fast speeds. The only speed limitations are the pin diode switches and the digital divider circuits, both of which can switch in under 1 microsecond. Many manufacturers of commercial test equipment use a mix & divide design for their synthesizers and they report that excellent phase noise and spurious performance can be achieved with adequate physical / electrical isolation between the stages. The major drawback for this scheme is the sheer size and power that would be required to make a synthesizer of this type for our application. The frequency resolution that is required for the EHF waveform would necessitate a very large number of cascaded mix and divide stages.

C - Direct Digital Synthesis

The Direct Digital Synthesizer (DDS) is a technology that has been around since the early 1970's.[3] A block diagram of a typical DDS is shown in Figure 1. The two major components of the DDS are a Numerically Controlled Oscillator (NCO)[4] and a Digital-to-Analog Converter (DAC). The NCO consists of the adder-register pair (also called a phase accumulator) and the ramp-to-sine wave lookup ROM. The output of the DDS is related to the phase accumulator input by the following equation:

$$f_{out} = \frac{Increment}{2^N} * f_{clock}$$

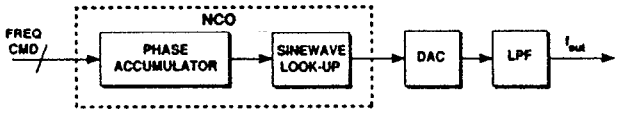

Figure 1 - Direct Digital Synthesizer.

The DDS typically provides a low frequency output with extremely high resolution and excellent frequency switching speed. The resolution of a DDS can be made arbitrarily small with very little additional circuitry or added circuit complexity. The switching time of a DDS is a function of the propagation delay through the digital gates and the settling time of the DAC, and is typically within a few clock cycles. Due to sampling theory a DDS can only generate frequencies up to a maximum of 1/2 the clock rate of the digital circuitry. Practically speaking, the useful output of a DDS is limited in bandwidth to a range approximately between 10% and 40% of the clock rate. This is due to both the anti-alias lowpass filter that necessarily follows the DAC and the bandpass filter that is required after any upconversion, i.e. DDS output frequencies near DC are difficult to process after an upconversion. (These limitations of narrow bandwidth and low output frequency can be overcome with bandwidth expansion techniques that are described in the next section.) The primary disadvantage of most direct digital synthesizers is the typically high spurious content caused by quantization and linearity limitations in the DAC. A very rough rule of thumb is that the spurious levels generated by DAC quantization equals 6 dB times the number of input bits (e.g. an 8 bit DAC would have quantization spurious 48 dB lower than the carrier). However, as the DAC is clocked at frequencies approaching its upper limit, spurs caused by non-linearities in the DAC become dominant. Therefore, using a DDS for a synthesizer in an EHF system requires a careful understanding of the spurious performance to be expected from the DAC and the system level requirements.

The synthesizer architecture that is described in the remainder of this paper is a novel combination of a direct digital synthesizer and direct analog techniques.

III. Bandwidth Expansion for DDS

A basic limitation of any direct digital synthesizer is the available bandwidth. As was discussed above, the output tuning range of a DDS is less than 1/2 the clock rate of the digital circuitry. In order to increase the frequency coverage to the range that is required for the EHF waveform, some method of bandwidth expansion must be employed. Two of the basic techniques for expanding the tuning range available at the synthesizer output are frequency multiplication and offset mixing".

A - Frequency Multiplication

Frequency multiplication is the most simple method for obtaining bandwidth expansion. Putting the output of any portion of a synthesizer with a bandwidth B into a times n multiplier yields a bandwidth of (n * B) at the output of the multiplier, along with an associated reduction in resolution of 1/n. The primary disadvantage of multipliers is that phase noise and spurious from the DDS get enhanced by a factor of 20 log (n) dB as a side product of the multiplication.[5] This can put a severe limitation on system performance. As a basic ground rule when using a DDS, it is prudent to limit the amount of frequency multiplication to a minimum in order to maintain a clean output signal.

B - Offset Mixing

Bandwidth expansion by offset mixing" is schematically represented in Figure 2. A DDS, which has a tuning range of Δf, is mixed with a pure tone. This tone is a single frequency selected from a set of harmonics, which are spaced at Δf. (These harmonics are typically produced by a comb generator.) By mixing the DDS with adjacent harmonics, an output bandwidth is produced which is an integral number of times broader than the DDS alone. The example in Figure 2 shows four harmonics that are mixed with a DDS to yield an output tuning range that is four times as wide as the DDS alone.

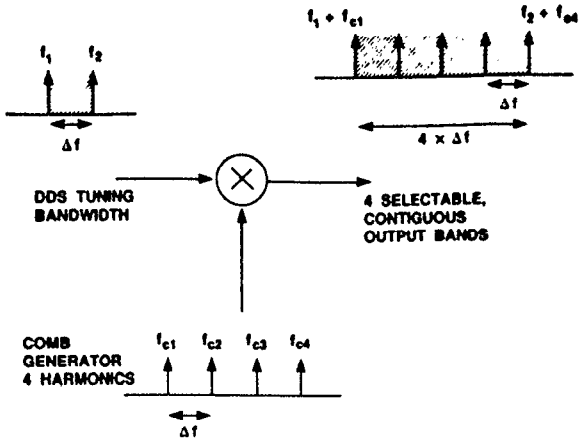

Figure 2 - Bandwidth Expansion by Offset Mixing.

An effective, simple method of selecting a desired harmonic for offset mixing is to use a switchable filter bank (see Figure 3). A set of n bandpass filters is designed so that only one of the harmonics of the comb generator can pass through any one particular filter. Two n-way switches are used to route the set of harmonics from the comb generator through the appropriate filter in the filter bank, resulting in a single frequency which is then applied to the offset mixer.

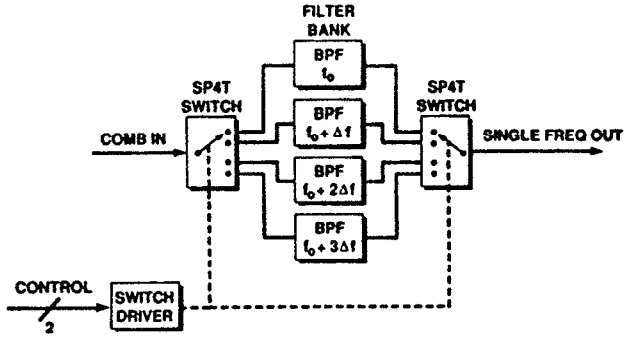

Figure 3 - Switched Filter Bank.

GaAs Fet switches built on MMIC circuits have become readily available within the last two years. These can be used as the switching elements in the filter bank instead of the more common PIN diodes. The FET's can switch as fast as PIN diodes and since only gate voltage is applied to the FET (instead of forward current in the diodes), the drive circuitry requires virtually no power consumption.

IV. Frequency Generator Design Description

A general block diagram of the hybrid direct digital / direct analog frequency synthesizer is shown in Figure 4. The fundamentals of the circuitry for the DDS and bandwidth expansion have already been described. The frequency translation, or upconversion stages, are required to center the synthesizer output into the desired frequency band. The fixed frequencies generator sets the phase noise for the synthesizer, as well as generating the clock frequency for the DDS, the harmonics for the bandwidth expansion and the fixed frequencies for the upconversion stages.

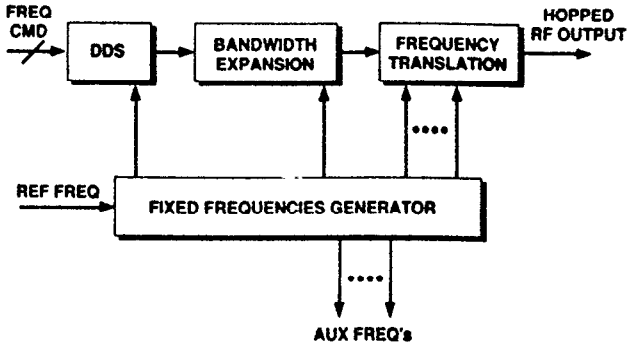

Figure 4 - Hybrid Direct Digital / Direct Analog Architecture.

The degrees of freedom in designing this synthesizer were bounded by the requirement to make the output compatible with the frequency plans of the Lincoln Laboratory Advanced SCAMP man-portable terminal and some other existing terminals.

The frequency plan of the synthesizer is shown in Figure 5. The design is based on a Direct Digital Synthesizer (DDS) comprising of Stanford Telecommunication's ECL numerically controlled oscillator (NCO) and Honeywell's digital to analog converter (DAC). The DDS is clocked at 300 MHz and is tuned over a 50 MHz frequency range. The DDS is followed by a frequency doubler yielding a 100 MHz bandwidth. A six-channel, switched filter bank in combination with a 100 MHz comb generator provides the required bandwidth expansion to 600 MHz of tuning range. The remaining mixers were chosen to minimize spur generation while converting the output to the proper frequency band.

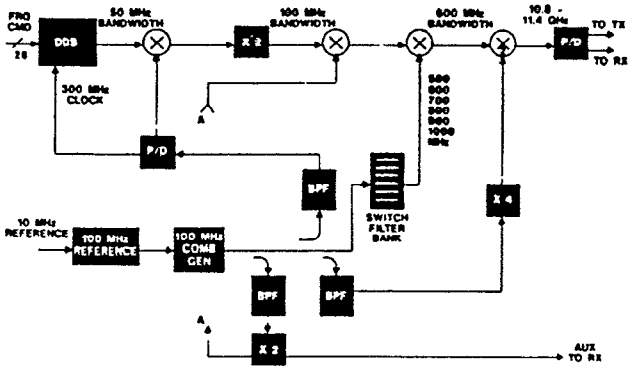

Figure 5 - RF Generator Frequency Plan.

The single-pole, six throw switches are proprietary MIC hybrids, developed at Lincoln Laboratory, that use Anzac

GaAs MMIC switches with CMOS driver circuitry, for low power consumption. The 100 MHz comb generator was designed by using a Giga-Bit Logic GaAs digital IC to generate a pulse train with a 300 picosecond pulse width and a 10 nanosecond repetition rate. This proprietary design eliminates the need for a step recovery diode (SRD) comb generator and requires no tuning or alignment. Designing both the bandwidth expansion harmonic generator and the LO distribution network to be multiples of 100 MHz greatly simplified the circuitry required, thereby keeping the size and dc power dissipation to a minimum. Commercially available GaAs MMIC amplifiers are used in the upconversion stages between 2 - 12 GHz.

A large emphasis in this project has been placed on achieving a small mechanical package for this synthesizer. The size of the complete synthesizer is 6.5 x 5.5 x 2.0 inches (71.5 cubic inches) and it weighs 3.0 pounds. This is a significant achievement in comparison to other synthesizers for EHF terminals, being smaller and lighter (to this author's knowledge) than any other synthesizer currently being made for this type of application. The synthesizer is housed in two separate modules, where each module can be assembled and tested independently. A photograph of the two modules is shown in Figure 6.

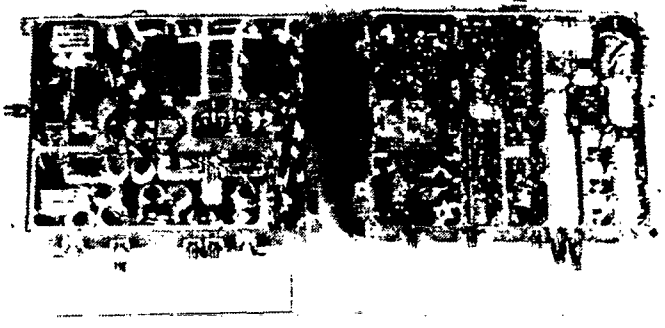

Figure 6 - Advanced SCAMP Frequency Generator.

V. Synthesizer Performance Evaluation

The critical parameters for this synthesizer are: a) frequency resolution and tuning bandwidth, b) frequency switching speed, c) worst case spurious and phase noise, and d) output power over frequency and temperature.

The resolution of this synthesizer is ~ 2.2 Hz and is set by the Direct Digital Synthesizer's 300 MHz clock and its 28 bit increment word, as described in Section II. By virtue of the design of the frequency expansion circuitry and upconversion stages, the output of the synthesizer can be tuned anywhere between 10.8 GHz and 11.4 GHz (also see Figure 10).

The frequency switching speed and settling time were measured by hopping the synthesizer between two frequencies and mixing the output with a CW version of one of the two frequencies. This mixer acts as a phase detector and the synthesizer is considered settled when its output comes within a few degrees of the final value. Figure 7 is a plot of the output of the phase detector and shows that the synthesizer has settled in under 500 nano-seconds.

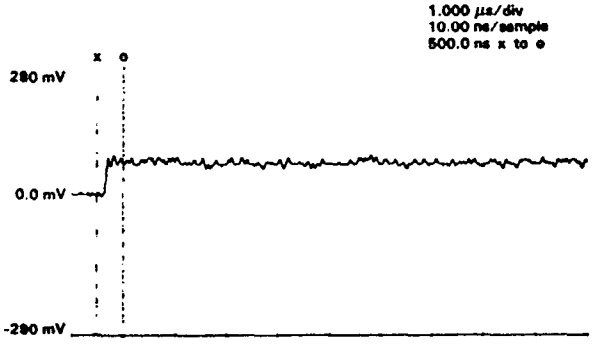

Figure 7 - Switching Speed Performance.

The dominant spurious signals in the synthesizer's output are generated by the DAC in the DDS and by Manley-Rowe products in the upconversion stages. The output frequency which had the worst case spurious was found by analysis and verified by extensive testing. The spectrum for this output signal is shown in Figure 8. The largest, single spur is 40 dB lower than the carrier at the 11 GHz output. The single-sided phase noise, L(f), of the synthesizer is shown in Figure 9 and measures -80 dBc/Hz at 1 kHz offset from the carrier.

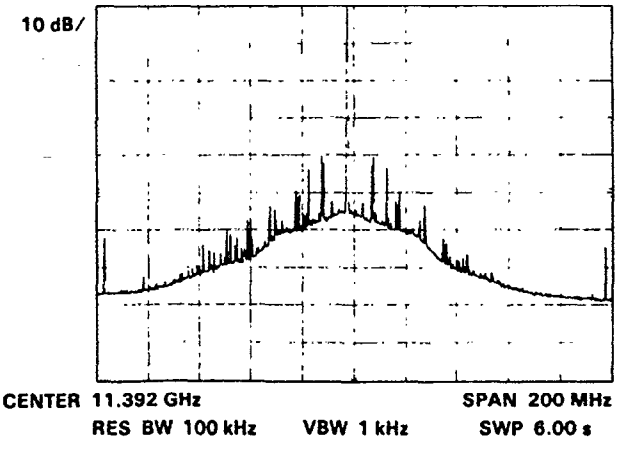

Figure 8 - Spurious Performance.

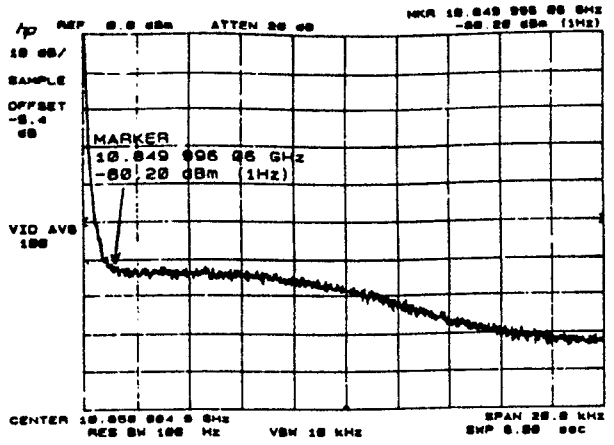

Figure 9 - Phase Noise Performance.

A plot of the synthesizer's output power is shown in Figure 10 and demonstrates the 600 MHz bandwidth coverage. The peak to peak variation in output power over frequency is less than 4 dB pk-pk.

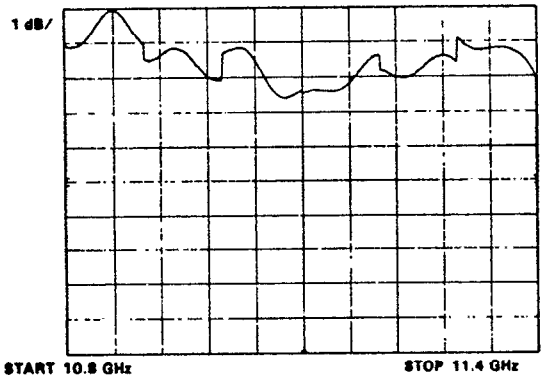

Figure 10 - Output Power vs. Frequency.

VI. Conclusions

A frequency generator system has been described that was designed using a novel mixture of direct digital and direct analog synthesizer techniques. The size and performance of this new synthesizer makes it very well suited for the class of man-portable EHF terminals, similar to the Advanced SCAMP being developed at Lincoln Laboratory. The implementation of this design approach is seen as an important step towards the miniaturization of EHF communications hardware.

Acknowledgments

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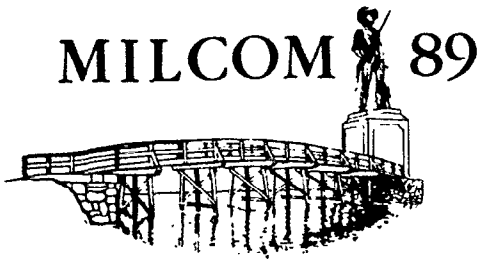

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